Impact of Intrinsic Channel Scaling on InGaAs Quantum-Well MOSFETs

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***Abstract*— Using a novel gate-last process scheme that affords precise channel thickness control, we have fabricated self-aligned InGaAs quantum-well (QW) MOSFETs. Devices with a channel thickness between 3 and 12 nm, and a gate length between 40 nm and 5 μm are fabricated on a heterostructure that includes a composite InGaAs/InAs QW and an InP barrier. It is observed that channel thickness has a strong impact on the device characteristics. In general, a thick channel is beneficial to ON-state figures of merit, including transconductance and effective carrier mobility. However, a thin channel is beneficial to OFF-state metrics, such as subthreshold swing and drain-induced barrier lowering (DIBL). The InAs composition and effective mass that electrons experience in the channel emerges as a factor that significantly affects channel mobility and presumably the transport characteristics of these devices. The subthreshold swing and DIBL are found to follow a classic scaling behavior. This suggests that the InGaAs QW MOSFETs are at the limit of scaling around $L_g = 50$ nm.**

***Index Terms*— III–V, MOSFETs, quantum-well (QW), self-aligned.**

I. Introduction

InGaAs is a promising candidate as an n-type channel material for future CMOS due to its superior electron transport properties [1], [2]. Great progress has recently taken place in demonstrating InGaAs MOSFETs. Several self-aligned device architectures have been demonstrated, such as recessed gate [3], [4], implanted source and drain (SD) [5], [6], regrown SD [7], [8], and metallic SD [9], [10]. Among the self-aligned InGaAs MOSFET architectures, the recessed-gate design is an attractive option due to its scalability and simplicity. Recessed-gate InGaAs MOSFETs have delivered the smallest SD contact spacing (footprint) and the smallest contact size of 40 nm in a tight-pitch MOSFET array prototype [11].

High-performance recessed-gate InGaAs MOSFETs are characterized by low parasitics and a simple channel geometry. This has enabled the fundamental device physics studies of relevance for future logic. For example, we have recently identified the band-to-band tunneling amplified by a parasitic bipolar effect as the cause of excess OFF-state leakage current at high drain bias in InGaAs MOSFETs [12], [13]. Mitigating this is an important priority for future scaled InGaAs MOSFETs [7], [14], [15].

In this quest, there has been increasing concern about transport characteristics being degraded by an aggressive structural design directed to mitigate short-channel effects (SCEs). Split-C–V measurements on long-channel devices have shown that the ultrathin channels suffer from significant mobility degradation [16]. This can be the result of increased scattering and a heavier carrier effective mass from a thinner channel [16]. These mechanisms will also affect short-channel transistors with gate lengths comparable with the mean-free-path, or close to the ballistic limit. However, to date, there have been few experimental studies on the high-performance InGaAs MOSFETs of different channel thicknesses with gate lengths that span from the drift-diffusion regime to the ballistic transport regime, and address both carrier transport and SCE control. Our device technology demonstrated in [11] allows us to tightly control the channel thickness through a precision recess method. At the same time, the gate length of functional devices can be scaled down to 40 nm. This device technology then represents an ideal platform to study the tradeoffs involved in a channel thickness design as the gate length is scaled.

This paper is organized as follows. In Section II, we briefly describe the key features of our transistor and its fabrication process, particularly the engineering scheme that we use to achieve precise channel thickness control. In Sections III and IV, we show the impact of intrinsic scaling on ON-state and OFF-state characteristics. This includes both the channel thickness (vertical) scaling and the gate length (lateral) scaling. We finally state our key conclusions in Section V. This paper refines and extends the experimental study in [11].

II. Device Fabrication

A cross-sectional schematic of a typical device used for this paper is shown in Fig. 1. This schematic shows a surface-channel design, in which the n^+ cap structure has been recessed to expose the quantum-well (QW) channel. A buried-channel design is also possible if the etching does not completely remove the thin InP barrier (also behaving as etch-stop) above the as-grown channel.

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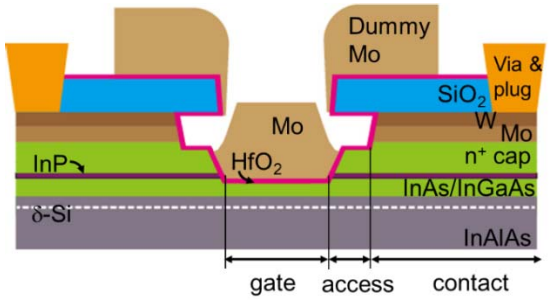

Fig. 1. Cross-sectional schematic of a self-aligned surface-channel InGaAs QW-MOSFET fabricated for this paper. Buried-channel designs are also possible by leaving the InP barrier above the channel in the intrinsic gate portion of the device.

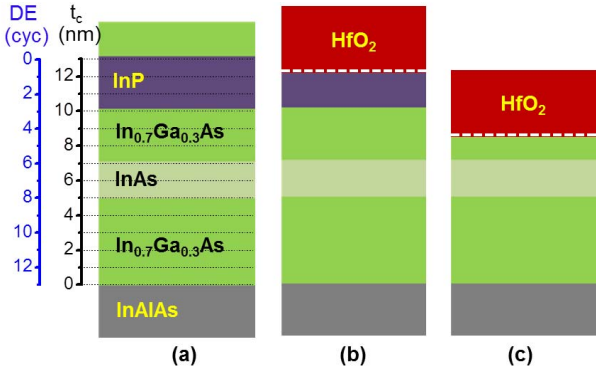

Fig. 2. (a) Correlation between the number of digital etch cycles and the final channel thickness. Examples of (b) buried channel and (c) surface channel designs. Dashed lines beneath the HfO_2: location of the oxide/semiconductor interface.

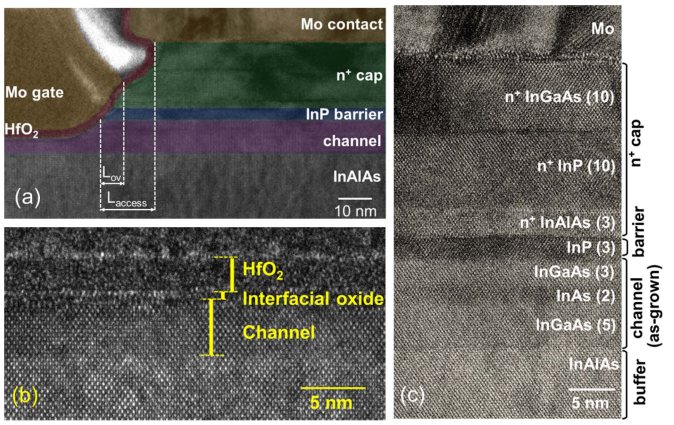

Fig. 3. (a) False-color TEM cross section of a finished QW-MOSFET around the edge of the gate. The final channel thickness of this device is 4 nm. The access region (L_{access}) and gate-n^+ overlapping region (L_{ov}) are indicated. (b) HRTEM cross section of the intrinsic gate region. (c) HRTEM of the contact region. Bracket after layer label indicates thickness in nanometers.

The devices are fabricated by a self-aligned process as reported in [11] and in more detail in [17]. A simplified description is given here. The heterostructure is grown by molecular beam epitaxy on an InP substrate and it comprises from bottom to top of a ~400-nm-thick InAlAs buffer with a Si δ-doped sheet placed 5 nm beneath the channel, an undoped $In_{0.7}Ga_{0.3}As/InAs/In_{0.7}Ga_{0.3}As$ channel with a layer thickness of 5/2/3 nm, a 3-nm undoped InP barrier, and a composite n^+ cap containing n^+ InAlAs, n^+ InP, and n^+ $In_{0.7}Ga_{0.3}As$. The Si doping level in the cap is between 2×10^{19} and 3×10^{19} cm^{-3}. Unless indicated, all layers are lattice matched to the InP substrate.

Device fabrication begins with a blanket deposition of 15-nm sputtered Mo, 15-nm sputtered W, and 50-nm CVD SiO_2. E-beam lithography is used to define the gate region. SiO_2, W, and Mo are then sequentially etched using F-based reactive ion etching (RIE), which also requires a proper annealing to repair the RIE damage [18]. In this process, an overhang is created that defines the length of the access region.

The III–V cap recess is then performed. The III–V layers are first recessed by a Cl-based RIE [15], followed by digital etch. The III–V RIE is self-aligned to the SiO_2 hard mask, and stops a few nanometers above the InP barrier. The digital etch is made of two steps: 1) oxide formation by low power O_2 plasma and 2) oxide stripping by dilute sulfuric acid. When separated, both steps are self-limiting and, under our selected conditions, they remove ~1 nm of semiconductor materials per full cycle [19].

After the last cycle of digital etch, a fresh semiconductor surface is exposed, immediately after which, 2.5-nm HfO_2 is deposited as a gate insulator by atomic layer deposition (ALD), followed by Mo gate electrode evaporation. The device is completed with gate patterning, via opening, and metal pad deposition.

Accurate channel thickness control is the heart of this study. To realize this, during the digital etch, we use a procedure that allows us to pinpoint the precise location of the top surface of the InP etch-stop layer [17]. From that point on, we can calculate the number of digital etch cycles needed to achieve a target channel thickness. Here, we use t_c to denote the total channel thickness left after the III–V recess, that is, the total semiconductor thickness above the InAlAs buffer in the intrinsic region of the device. The correlation between the number of digital etch cycles and the final channel thickness, and the examples of buried channel and surface channel designs are shown in Fig. 2(a)–(c). For t_c between 11 and 13 nm, the high-κ dielectric interface is located on the InP barrier, resulting in a buried channel device [Fig. 2(b)]. For t_c of 10 nm or below, the high-κ dielectric directly lies on the QW channel, resulting in a surface channel device [Fig. 2(c)]. For t_c below 5 nm, the high-mobility InAs core in the channel is entirely removed. The estimated t_c involves 1-nm uncertainty due to the discrete nature of our digital etching technique [19].

Fig. 3(a) shows a cross-sectional transmission electron microscopy (TEM) image of the transition region between the intrinsic channel on the left and the extrinsic region on the right in a finished device with $t_c = 4$ nm. False color has been added to highlight the different layers. The access region is defined as the spacing (L_{access}) between the edge of the intrinsic channel and the edge of the contact. For this device, L_{access} is 15 nm. Within this small access region, a gate-n^+ overlap region (L_{ov}) is created by introducing a slight angle and sample rotation during gate evaporation. L_{ov} spans a lateral dimension of ~7 nm. The actual n^+-gate

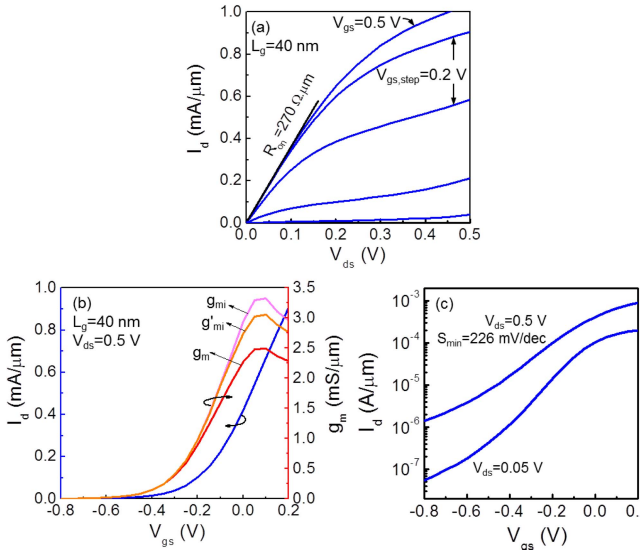

Fig. 4. Electrical characteristics of device with $t_c = 9$ nm and $L_g = 40$ nm. (a) Output characteristics. (b) Transfer and transconductance characteristics at $V_{ds} = 0.5$ V. (c) Subthreshold characteristics. In (b), extrinsic transconductance is labeled as g_m, intrinsic transconductance based on first-order model as g_{mi}, and intrinsic transconductance with output conductance correction as g'_{mi}.

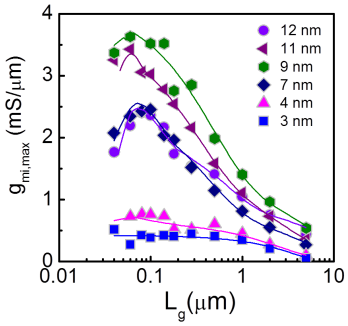

Fig. 5. Peak intrintsic transconductance at $V_{ds} = 0.5$ V versus L_g for different t_c.

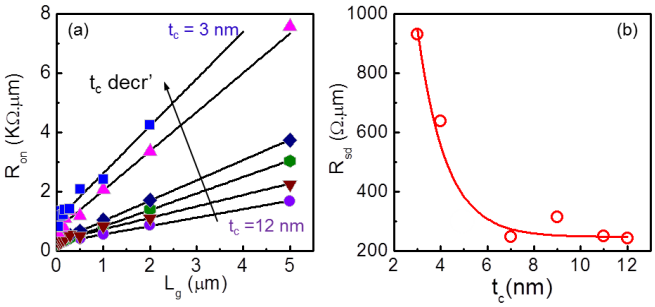

Fig. 6. (a) R_{ON} versus L_g for t_c from 3 to 12 nm, in which R_{sd} is extracted from the y-intersection. (b) R_{sd} versus t_c.

overlap distance is slightly longer due to the side-wall angle. This design with a short access region that partially overlaps with the gate saves device footprint, reduces parasitic series resistance, and maintains sufficient isolation between the gate and the SD contacts.

Fig. 3(b) and (c) are the high-resolution TEM (HRTEM) images for the intrinsic gate region and the extrinsic contact region, respectively. Fig. 3(b) shows that a uniform channel and a flat surface are obtained after the III–V recess. The channel is between 7 and 8 atomic monolayers thick. This agrees with our targeted channel thickness for this device of 4 nm and showcases the excellent accuracy of our process. The 2.5-nm HfO_2 gate dielectric is also highlighted. Between the dielectric and the channel, an interfacial oxide of 0.5–1 nm is observed. This is probably formed during the transition between the last native oxide stripping and the ALD. It has been reported that ALD-HfO_2 using TEMAH precursor, as is the case here, results in a self-cleaning effect on the InGaAs surface. This refers to the partial removal of the native oxide, which mitigates Fermi-level pinning at the HfO_2/InGaAs interface [20]. In our case, some residual native oxide appears to remain at the InGaAs interface. Electron trapping defects in this interfacial layer might result in V_t instability after the prolonged gate stress [21]. Fig. 3(c) also shows the Mo ohmic contact on InGaAs. A smooth, unalloyed contact interface free of any interfacial oxide is evident.

III. ON-State Characteristics

Electrical characteristics of a short-channel transistor are shown in Fig. 4. This device has $t_c = 9$ nm (surface-channel) and $L_g = 40$ nm. The output characteristics in Fig. 4(a) show an excellent ON-resistance of 270 $\Omega \cdot \mu$m. At $V_{ds} = 0.5$ V, the transconductance and subthreshold characteristics in Fig. 4(b) and (c) show a peak extrinsic transconductance ($g_{m,\max}$) of 2.5 mS/μm and a minimum subthreshold swing ($S_{\min}$) of 226 mV/decade. Due to the relaxed channel thickness and the extremely short channel of this device, a significant SCE is observed. A systematic study on SCE will be discussed later. In the same chip, a hero device with $L_g = 80$ nm delivers a record $g_{m,\max}$ of 3.1 mS/μm and R_{ON} of 190 $\Omega \cdot \mu$m [11].

We select the intrinsic peak transconductance ($g_{mi,\max}$) as the metric to study the scaling behavior of ON-state performance. The intrinsic transconductance (g_{mi}) is estimated using the method in [22]. Here it does not take into account the effect of the output conductance because the worst case (highest output conductance) of the shortest gate length device with the thickest channel, this correction resulted in a relative small error (8%) in the estimation of $g_{mi,\max}$ as shown in Fig. 4(b). Fig. 5 graphs $g_{mi,\max}$ versus L_g for families of devices with different t_c. We find that $g_{mi,\max}$ follows a classic gate length scaling behavior: it increases as L_g decreases and it eventually saturates. For $t_c > 7$ nm, $g_{mi,\max}$ decreases as the gate length further decreases. This is the result of a significant SCE.

In extracting g_{mi}, we use the measured source resistance R_s. This is obtained from a measurement of the ON resistance (R_{ON}), which is performed at a high gate overdrive of 0.8 V. Fig. 6(a) shows R_{ON} as a function of L_g for t_c from 12 to 3 nm. For all t_c values, a linear dependence of R_{ON} with L_g is obtained. The intercept of these lines with the y-axis gives the value of R_{sd}, the sum of the SD resistance. Fig. 6(b) shows R_{sd} as a function of t_c. $t_c > 7$ nm devices exhibit R_{sd} of $\sim$250 $\Omega \cdot \mu$m independent of t_c. This excellent result is due to our n^+-gate overlap design and good contact resistance [23]. For thin channels, R_{sd} rapidly increases as t_c reaches 4 nm and below. This is presumably due to the increased spreading resistance associated with the link region at the gate edge of

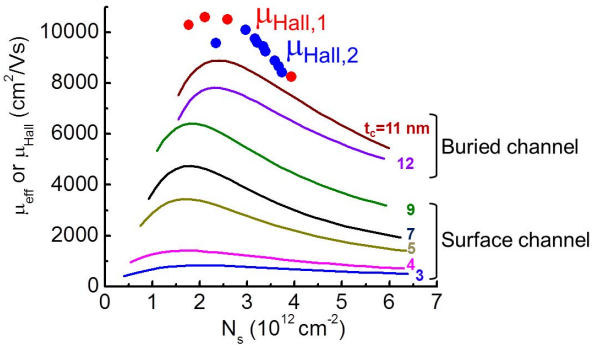

Fig. 7. Mobility versus sheet charge density. Continuous lines: effective channel mobility in long-channel devices ($L_g = 5\ \mu$m) with different channel thicknesses. Solid symbols: two sets of etch-Hall mobility from two growth test structures (see text).

the channel. Further investigation is required to understand this behavior. Due to the symmetry of the device, we assume that R_s is half of R_{sd}.

Fig. 5 reveals that the carrier transport in the intrinsic device is greatly influenced by t_c. The highest $g_{mi,\max}$ is obtained for $t_c = 9$ nm, which is the thickest surface-channel device that we have fabricated. For the channels thicker than this, the devices are of buried-channel type and $g_{mi,\max}$ decreases due to a loss in gate-channel capacitance [11]. For the channels thinner than this, $g_{mi,\max}$ rapidly decreases. This reveals worsening transport characteristics.

Independent evidence of the key role of transport in the performance of these devices is obtained from the measurements of channel mobility. The effective field mobility, μ_{eff}, is extracted by the split-C–V method in long-channel devices ($L_g = 5\ \mu$m) and the results are shown in Fig. 7 as a function of sheet electron concentration (N_s). The I_d–V_{gs} characteristics used in the mobility extraction were corrected for series resistance. This correction is relatively small: in the worst case (highest N_s at thick t_c), it is 14%. The impact of carrier trapping is not considered. It has been reported that a high concentration of border traps can exist in the high-κ oxide close to the III–V interface and causes significant trapping especially at high gate voltage [24], [25]. This could lead to error in the mobility extraction at a high carrier concentration.

Fig. 7 also includes the measurements of Hall mobility versus a sheet electron concentration from two epi calibration test structures that were grown immediately before the actual device heterostructures. These test samples have the same channel and barrier design as the device heterostructure but a modified cap that consists of n^+ InAlAs (3 nm), n^+ InP (3 nm), and n^+ $In_{0.53}Ga_{0.47}As$ (25 nm) with Si doping between 2×10^{19} and 3×10^{19} cm^{-3}. Hall mobility measurements are performed as the n^+ InGaAs portion of the cap is thinned down through selective wet etching. This results in a reduction of N_s and an increase in mobility as the relative fraction of charge in the high-mobility channel increases. A heterostructure with a high Hall mobility has been found to be essential to obtaining a high effective channel mobility of III–V MOSFET. Our results confirm this observation.

Fig. 7 reveals a nearly progressive deterioration of channel mobility as the channel is thinned down. The highest

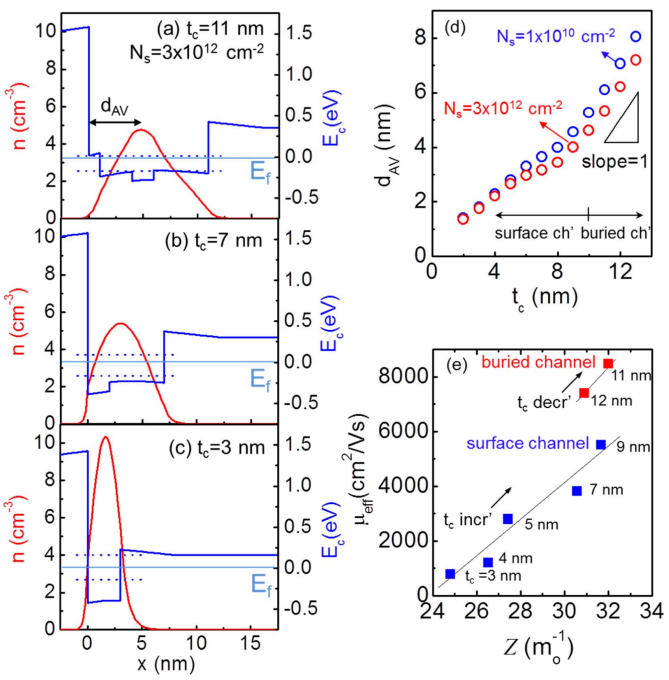

Fig. 8. (a)–(c) Carrier distribution (n) and conduction-band energy (E_c) in the direction perpendicular to the channel. The semiconductor/oxide interface is placed at $x = 0$. The energy of the first two quantum states is shown in dashed lines. (d) Average distance of channel electron population (d_{AV}) with respect to the oxide–semiconductor interface at N_s of 1×10^{10} cm^{-2} (blue) and 3×10^{12} cm^{-2} (red). The schematic of d_{AV} is shown in the inset in (a). (e) Experimental mobility versus Z at N_s of 3×10^{12} cm^{-2} (see text).

peak mobility is obtained in the buried channel device with 1-nm InP barrier where $\mu_{\text{eff}} = 8800$ cm^2/V · s at N_s of 2.6×10^{12} cm^{-2}. This is ~80% of the etch-Hall mobility at the same carrier concentration. With an InP barrier of 2 nm, the mobility is slightly lower. In the surface channel devices, the mobility is lower than in the buried-channel designs and it monotonically drops as the channel becomes thinner. The mobility rapidly falls when t_c is reduced below 5 nm.

In order to understand these results, we have performed 1-D Poisson–Schrödinger (P–S) simulations (Nextnano^3 [27]) in the intrinsic region of the device. Fig. 8(a)–(c) shows the carrier distribution (n) and the conduction-band edge energy (E_c) in the direction perpendicular to the channel (x) at a sheet electron concentration of $N_s = 3 \times 10^{12}$ cm^{-2} for t_c of 11, 7, and 3 nm. For a thick channel, the charge in the channel is broadly spread in space and away from the oxide–semiconductor interface. In a very thin channel, the electrons are tightly confined against the interface.

In order to evaluate the role of the charge distribution on transport, we have calculated the distance of the charge centroid in the channel from the oxide–semiconductor interface, d_{AV}. This is graphically indicated in Fig. 8(a) and is computed using the following expression:

$$d_{AV} = \frac{1}{N_s} \int_0^{t_c} n(x) \cdot x dx. \tag{1}$$

In this equation, $n(x)$ is the local carrier density at a depth x from the oxide–semiconductor interface where $x = 0$.

Fig. 8(d) graphs d_{AV} as a function of t_c at N_s of 1×10^{10} and 3×10^{12} cm^{-2}, which are the scenarios close to threshold and for ON-state, respectively. It is clear that as the channel thickness increases, the charge centroid continuously moves further away from the metal–oxide interface. The trend is more pronounced for buried channels. From these calculations, we can conclude that in thin channel designs, the electrons suffer more from surface roughness scattering as well as remote columbic scattering, both of which would degrade the mobility.

The electrons in the InAs core possess the lowest effective mass and hence the higher mobility. The larger the electron fraction in the InAs subchannel, the higher the overall mobility should be. To quantitatively evaluate this, we extract the weighted average of the inverse of the Γ-valley effective mass (m_Γ) of the channel electron, Z, in the unit of m_o^{-1}. We obtained this from P–S simulations using

$$Z = \sum_i \frac{1}{m_i} \frac{1}{N_s} \int_{t_i} n(x) dx. \tag{2}$$

In this equation, the integrals evaluate the sheet electron concentration in the respective channel layer i, which can be InP and InAs or $In_{0.7}Ga_{0.3}As$. m_i and t_i are the effective mass and the thickness of channel layer, respectively. Effective mass of those materials follows the room-temperature values in [28].

Fig. 8(e) graphs experimental channel mobility versus Z, both at N_s of 3×10^{12} cm^{-2}. The figure reveals a clear correlation: increased Z results in higher mobility. Among the surface channel devices, the mobility monotonically increases with Z, which itself increases with t_c. This reflects the reduced effective mass and weaker alloy scattering associated with a higher relative InAs mole fraction in the channel. At a particular value of Z (~31), there is a step increase in the mobility for the buried-channel designs. This is likely due to the reduction of interface scattering experienced by the electrons due to increased distance of the 2DEG from the oxide interface. As can be observed in Fig. 8(d), the 2DEG is close to the HfO_2/III–V interface for the surface channel devices, and it rapidly moves away from the HfO_2/III–V interface in the buried channel devices. However, in those devices, increased t_c brings about increased penetration of the electron wave function into the InP barrier, which results in a reduction of Z. This is the likely reason why now mobility decreases with increasing t_c from 11 to 12 nm.

The channel thickness dependence of the mobility contributes to explaining the strong impact that a channel thickness has on transconductance (Fig. 5). A complete model for the transconductance requires the development of a charge-control model and a transport model that consider the effective mass under strain in each of the channel layers and include conduction band nonparabolicity. This detailed study is best done on devices with a simpler channel design than those in this paper.

IV. OFF-State Characteristics

Despite the advantages of using a thick channel from a transport point of view, the drawback is evident in poor SCE control. Fig. 9(a) and (b) shows minimum subthreshold swing, $S_{\min}$, at $V_{ds} = 0.5$ V and drain-induced barrier lowering (DIBL) versus L_g for devices with varying t_c. DIBL is obtained from V_t shift between $V_{ds} = 0.05$ and 0.5 V at a constant current of $I_d = 1 \times 10^{-6}$ A/μm. However, not all devices can be turned OFF to this current level; hence some data points at short gate lengths are not available. $S_{\min}$ and DIBL in Fig. 9(a) and (b) follow a classic scaling behavior; they are both independent of gate length for long L_g but rapidly degrade as L_g scales down beyond a certain value. The onset of $S_{\min}$ and DIBL degradation occurs at longer gate lengths for the devices with thicker t_c.

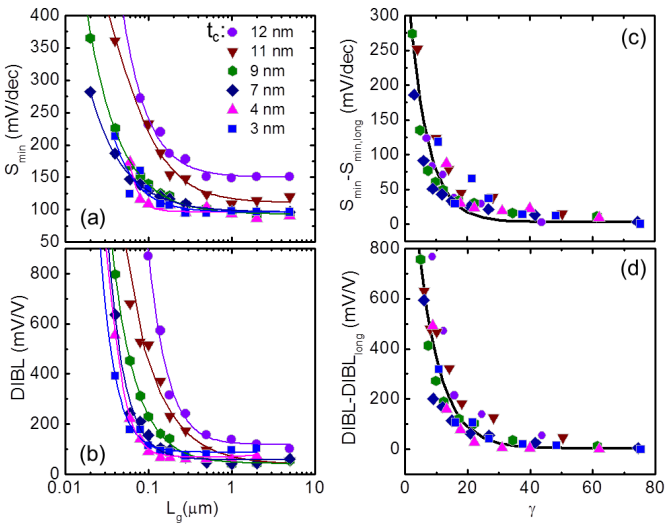

Fig. 9. (a) and (b) Experimental $S_{\min}$ and DIBL as a function of gate length for $t_c = 3$ to 12 nm. (c) and (d) $S_{\min}$–$S_{\min,\text{long}}$ and DIBL-DIBL$_{\text{long}}$ as a function of γ based on the natural channel length methodology discussed in the text.

These results can be analyzed using classic SCE electrostatics originally developed for fully depleted (FD) SOI MOSFETs in [29]. Electrostatically, the QW-MOSFETs discussed here are similar to FDSOI transistors, where the InAlAs buffer is equivalent to the buried oxide. Based on Yan's model, the natural channel length λ is defined that depends on the geometry and the dielectric constant of the various materials involved

$$\lambda = \sqrt{t_{\text{ins}} t_c \frac{\varepsilon_c}{\varepsilon_{\text{ins}}}}. \tag{3}$$

In this equation, ε_{ins} is the effective dielectric constant of the insulator and ε_c is that for the channel (both relative values); t_c is the channel thickness and t_{ins} is the effective insulator thickness. Here, we depart from Yan's model: in our case, ε_{ins} and t_{ins} consider the HfO_2 gate insulator, the interfacial oxide, and d_{AV}. For the interfacial oxide, we assume that it has a thickness of 1 nm (Fig. 3) and a relative dielectric constant of 16. The composition and properties of III–V native oxides are not well known. For example, relative dielectric constants between 9.9 and 23.3 have been reported for Ga_2O_3 [30], [31]. Here, we assume that the interfacial oxide has a dielectric constant given by the average of these two values. The average distance of channel electron away from the oxide–semiconductor interface, d_{AV}, arises from the quantum nature of the channel and the presence of the

InP barrier in the buried-channel designs. Here, we use d_{AV} at $N_s = 1 \times 10^{10}$ cm^{-2} as graphed in Fig. 8(d).

The scaling parameter γ that governs an SCE is the ratio of the effective channel length and the natural channel length

$$\gamma = \frac{L_{\text{eff}}}{\lambda} \quad (4)^1$$

where L_{eff} is related to gate length, but as argued below, it is not generally the same.

Fig. 9(c) and (d) shows the change of $S_{\min}$ and DIBL versus gate length, L_g, normalized by scaling length, λ. The data all nearly fall on top of each other suggesting a universal electrostatic scaling trend.

MOSFET designs with better SCE immunity start suffering from SCE degradation at smaller γ values. In Si FDSOI MOSFETs, it is reported that the well-designed device architectures maintain acceptable SCE down to γ of 5–10 [29], [32]. Reports on InGaAs HEMTs indicate SCE immunity down to $\gamma = 5$ [33]. In our device, we find that SCE FOMs start to degrade at $L_g/\lambda \sim 15$. This apparently early SCE degradation of our InGaAs MOSFETs might arise from two factors. First, here and in the analysis of III–V HEMTs [33], it is assumed that $L_{\text{eff}} = L_g$; but HEMTs have an underlapped SD, and therefore the physical gate length L_g is an underestimation of the effective channel length L_{eff}, and hence γ (4), while the MOSFETs in this paper, as with modern very large-scale integration transistors, are designed with a slight n^+-gate overlap, and therefore L_g is close to or a slight overestimation of the effective channel length.

Second, in our device, the introduction of an n-type δ-doped layer in the buffer below the channel is likely to degrade the subthreshold characteristics. This is equivalent to the introduction of positive fixed charge below the channel. In floating-body transistor designs, it has been observed that positive fixed charge beneath the channel results in degraded subthreshold characteristics in short III–V MOSFETs [3], [13] and FDSOI transistors [34]. This suggests that the appropriate transistor redesign might mitigate an SCE in future InGaAs QW-MOSFETs.

Our study reveals that planar InGaAs QW-MOSFETs, as fabricated here, even with the thinnest channels are at the limit of scaling at around $L_g \sim 50$ nm. As in Si MOSFETs, the use of 3-D device architectures can increase λ and allows the device to scale to even smaller L_g. In any case, this will require the use of a very thin semiconductor body. This suggests that the tradeoff between OFF- and ON-state performance will remain an important engineering challenge [11], [29].

V. Conclusion

We carry out a detailed vertical and lateral scaling study on InGaAs QW MOSFETs fabricated by a process that provides precise channel thickness control. We find that the intrinsic transconductance follows a classic gate length scaling behavior. The surface channel designs with a relatively thick channel provide the best transconductance characteristics. The buried-channel designs feature lower transconductance presumably due to a loss of gate capacitance. Thin channels suffer from severe transconductance degradation. From a study of channel mobility, we identify the effective mass in the channel as a key factor affecting transport characteristics. In contrast with their excellent ON-state performance, the OFF-state characteristics of thick channel devices are significantly compromised. We find that the subthreshold swing and DIBL follow a classic scaling behavior similar to that of the Si FDSOI MOSFETs. The current InGaAs QW-MOSFET is at the limit of scaling around $L_g \sim 50$ nm. This indicates the need for transistor redesign and advanced 3-D device architectures to deliver further progress.

[1] A factor of (1/2) is included in the original model. Here, it follows the definition without (1/2) for a similar study in [32] and [33].

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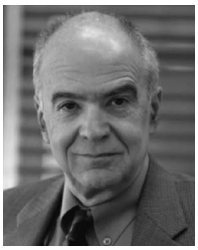

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